WHAT IS CLAIMED IS:

1. A semiconductor device having a multiple layered ridge, said ridge including:

a first semiconductor layer forming the bottom part of said ridge, said first semiconductor layer having a first etching speed in a first etchant;

a second semiconductor layer disposed above said first semiconductor layer, said second semiconductor layer having a second etching speed in the first etchant; and

a third semiconductor layer disposed above said second semiconductor layer and forming the top part of said ridge, said third semiconductor layer having a third etching speed in the first etchant,

wherein the second etching speed is higher than the first etching speed and slower than the third etching speed.

2. The semiconductor device according to claim 1, wherein said second semiconductor layer has a bottom surface located near the first semiconductor layer and top surface located near the third semiconductor layer, and wherein the second etching speed is variable and increases monotonically from the layer's bottom surface to the layer's top surface.

3. The semiconductor device according to claim 2, wherein the second etching speed increases continuously from the bottom surface of said second semiconductor layer to the top surface of said second semiconductor layer.

4. The semiconductor device according to claim 1, wherein said second semiconductor layer has a bottom surface located near the first semiconductor layer and top surface located near the third semiconductor layer, and wherein the second etching speed is variable and it increases in one or more steps from the layer's bottom surface to the layer's top surface.

5. The semiconductor device according to claim 2, wherein the second semiconductor layer comprises two or more atomic elements, and wherein the stoichiometric ratio of the atomic elements of said second semiconductor layer is changed to thereby make the second etching speed variable.

6. The semiconductor device according to claim 1, wherein said first semiconductor layer comprises a composition of $Al_{x1}Ga_{1-x1}As$ where the stoichiometric parameter x1 is substantially constant, wherein said third semiconductor layer comprises a composition of GaAs, and wherein said second semiconductor layer comprises a composition of $Al_{x2}Ga_{1-x2}As$ where the stoichiometric parameter x2 is a variable.

7. The semiconductor device according to claim 6, wherein the stoichiometric parameter x1 for the first semiconductor layer is in a range of 0.2 to 0.5.

8. The semiconductor device according to claim 1 further comprising an electrode layer disposed above said third semiconductor layer and covering at least a side of said ridge portion in the longitudinal direction, wherein

the thickness of said electrode layer is equal to or more than 100 nm.

9. The semiconductor device according to claim 1 wherein said second semiconductor layer has a thickness in a range of 5 nm to 1000 nm.

10. The semiconductor device according to claim 1 wherein said second semiconductor layer has a thickness in a range of 25 nm to 100 nm.

11. The semiconductor device according to claim 1 wherein said second semiconductor layer has a thickness in a range of 25 nm to 35 nm.

12. The semiconductor device according to claim 11 wherein the thickness of said first semiconductor layer is greater than the thickness of said second semiconductor layer, and wherein the thickness of the third semiconductor layer is greater than the thickness of the second semiconductor layer.

13. A method of manufacturing a semiconductor device having a multiple layered ridge, the method comprising the steps of:

forming a first semiconductor layer as a bottom part of the ridge, said first semiconductor layer being etched at a first etching speed by a first etchant;

forming a second semiconductor layer above said first semiconductor layer, said second semiconductor layer being etched at a second etching speed by the first etchant; and

forming a third semiconductor layer above said second semiconductor layer as a top part of the ridge, said third semiconductor layer being etched at a third etching speed by the first etchant,

wherein the second etching speed is higher than the first etching speed and slower than the third etching speed.

14. The method according to claim 13, wherein said second semiconductor layer has a bottom surface located near said first semiconductor layer and top surface located near said third semiconductor layer, and wherein said second semiconductor layer is formed with a composition that causes the second etching speed to be variable and to increase monotonically from the layer's bottom surface to the layer's top surface.

15. The semiconductor device according to claim 14, wherein the second etching speed increases continuously from the bottom surface of said second semiconductor layer to the top surface of said second semiconductor layer.

16. The method according to claim 13, wherein said second semiconductor layer has a bottom surface located near said first semiconductor layer and top surface located near said third semiconductor layer, and wherein said second semiconductor layer is formed with a composition that causes the second etching speed to be variable and to increase in one or more steps from the layer's bottom surface to the layer's top surface.

17. The method according to claim 14, wherein the second semiconductor layer comprises two or more atomic elements, and wherein the stoichiometric ratio of the elements of said second semiconductor layer is sequentially changed to thereby make the second etching speed variable.

18. The method according to claim 13, wherein said first semiconductor layer comprises a composition $Al_{x1}Ga_{1-x1}As$ where x1 is substantially constant, wherein said third semiconductor layer comprises a composition of GaAs, and wherein said second semiconductor layer comprises a composition of $Al_{x2}Ga_{1-x2}As$ where x2 is a variable.

19. The method according to claim 13 further comprising a step of forming an electrode layer above said third semiconductor layer and covering at least the side of said ridge portion in the longitudinal direction, wherein the thickness of said electrode layer is equal to or more than 100 nm.

20. The method according to claim 13 further comprising a step of forming an electrode layer above said third semiconductor layer and covering at least the side of said ridge portion in the longitudinal direction, wherein the thickness of said electrode layer is equal to or more than 150 nm.

21. The method according to claim 13 further comprising a step of forming an electrode layer above said third semiconductor layer and covering at least the

side of said ridge portion in the longitudinal direction, wherein the thickness of said electrode layer is equal to or more than 200 nm.

22. A semiconductor device having a multiple layered ridge formed at a first surface of a substrate, said ridge including:

a base attached to the substrate, an upper face located above the base, and at least a first side face located between the ridge's upper face and the base;

a first semiconductor layer located closer to the base than the upper face of the ridge, said first semiconductor layer having a composition of $Al_{x1}Ga_{1-x1}As$ where the stoichiometric parameter x1 is substantially constant;

a second semiconductor layer located above said first semiconductor layer and below said upper face, said second semiconductor layer having a composition of $Al_{x2}Ga_{1-x2}As$ where the stoichiometric parameter x2 is variable with a range of values which are less than or equal to X1; and

a third semiconductor layer located above said second semiconductor layer and below said upper face, said third semiconductor layer having a composition of $Al_{x3}Ga_{1-x3}As$ where the stoichiometric parameter x3 is substantially constant and substantially less than or equal to the lowest value of the stoichiometric parameter x2; and

wherein said second semiconductor layer has a bottom surface located near the first semiconductor layer and top surface located near the third semiconductor layer,

wherein the stoichiometric parameter X2 decreases monotonically from the bottom surface of the second semiconductor layer to the top surface of the second semiconductor layer, and

wherein said first side face comprises a forward mesa surface.

23. The semiconductor device according to claim 22, wherein said second semiconductor layer has a bottom surface located near the first semiconductor layer and top surface located near the third semiconductor layer, and wherein the stoichiometric parameter x2 decreases monotonically from the layer's bottom surface to the layer's top surface.

24. The semiconductor device according to claim 23, wherein the stoichiometric parameter x2 decreases continuously from the bottom surface of said second semiconductor layer to the top surface of said second semiconductor layer.

25. The semiconductor device according to claim 22, wherein said second semiconductor layer has a bottom surface located near the first semiconductor layer and top surface located near the third semiconductor layer, and wherein the stoichiometric parameter x2 decreases in one or more steps from the layer's bottom surface to the layer's top surface.

26. The semiconductor device according to claim 22, wherein said first side face comprises a concave surface.

27. The semiconductor device according to claim 22, wherein the stoichiometric parameter x1 for the first semiconductor layer is in a range of 0.2 to 0.5.

28. The semiconductor device according to claim 22, wherein the stoichiometric parameter x1 for the first semiconductor layer is in a range of 0.25 to 0.35.

29. The semiconductor device according to claim 22, wherein the stoichiometric parameter x1 for the first semiconductor layer is in a range of 0.2 to 0.5, and wherein the stoichiometric parameter x3 for the third semiconductor layer is less than or equal to 0.05.

30. The semiconductor device according to claim 22, wherein the third semiconductor layer comprises GaAs with the stoichiometric parameter x3 being substantially equal to zero.

31. The semiconductor device according to claim 22 wherein said second semiconductor layer has a thickness in a range of 5 nm to 1000 nm.

32. The semiconductor device according to claim 22 wherein said second semiconductor layer has a thickness in a range of 25 nm to 100 nm.

33. The semiconductor device according to claim 22 wherein said second semiconductor layer has a thickness in a range of 25 nm to 35 nm.

34. The semiconductor device according to claim 32 wherein the thickness of said first semiconductor layer is greater than the thickness of said second semiconductor layer, and wherein the thickness of the third semiconductor layer is greater than the thickness of the second semiconductor layer.

35. The semiconductor device according to claim 22 further comprising an electrode layer disposed above said third semiconductor layer and covering at least the side of said ridge portion in the longitudinal direction, wherein the thickness of said electrode layer is equal to or more than 100 nm.

36. The semiconductor device according to claim 22 further comprising an electrode layer disposed above said third semiconductor layer and covering at least the side of said ridge portion in the longitudinal direction, wherein the thickness of said electrode layer is equal to or more than 150 nm.

37. The semiconductor device according to claim 22 further comprising an electrode layer disposed above said third semiconductor layer and covering at least the side of said ridge portion in the longitudinal direction, wherein the thickness of said electrode layer is equal to or more than 200 nm.

38. A method of manufacturing a semiconductor device having a multiple layered ridge, the ridge having a base attached to a substrate, an upper face located above the base, and at least a first side face located between the ridge's upper face and the base, the method comprising the steps of:

(a) forming a first semiconductor layer located closer to the base than the upper face of the ridge, the first semiconductor layer having a composition of $Al_{x1}Ga_{1-x1}As$ where the stoichiometric parameter x1 is substantially constant;

(b) forming a second semiconductor layer over the first semiconductor layer and located below the upper face, the second semiconductor layer having a bottom surface adjacent to the first semiconductor layer and top surface opposite to the bottom surface, the second semiconductor layer having a composition of $Al_{x2}Ga_{1-x2}As$ where the stoichiometric parameter x2 is variable with a range of values which are less than or equal to x1, the second layer being formed such that the stoichiometric parameter x2 decreases substantially monotonically from the bottom surface of the second semiconductor layer to the top surface of the second semiconductor layer; and

(c) forming a third semiconductor layer over the second semiconductor layer and located below the upper face, the third semiconductor layer having a composition of $Al_{x3}Ga_{1-x3}As$ where the stoichiometric parameter x3 is substantially constant and substantially less than or equal to the lowest value of the stoichiometric parameter x2; and

(d) exposing selected portions of the first, second, and third semiconductor layers to a common

etchant to form the ridge such that at least a portion of the first side surface of the ridge has a slope of a forward mesa ridge.

39. The method of claim 38, wherein the second semiconductor layer is formed such that the stoichiometric parameter x2 decreases continuously from the bottom surface of said second semiconductor layer to the top surface of said second semiconductor layer.

40. The method of claim 38, wherein the second semiconductor layer is formed such that the stoichiometric parameter x2 decreases in one or more steps from the bottom surface of said second semiconductor layer to the top surface of said second semiconductor layer.

41. The method of claim 38, wherein the first side face comprises a concave surface.

42. The method of claim 38, wherein the stoichiometric parameter x1 for the first semiconductor layer is in a range of 0.2 to 0.5.

43. The method of claim 38, wherein the stoichiometric parameter x1 for the first semiconductor layer is in a range of 0.25 to 0.35.

44. The method of claim 38, wherein the stoichiometric parameter x1 for the first semiconductor layer is in a range of 0.2 to 0.5, and wherein the stoichiometric parameter x3 for the third semiconductor

layer is less than or equal to 0.05.

45. The method of claim 38, wherein said second semiconductor layer has a thickness in a range of 5 nm to 1000 nm.

46. The method of claim 38, wherein said second semiconductor layer has a thickness in a range of 25 nm to 100 nm.

47. The method of claim 38, wherein said second semiconductor layer has a thickness in a range of 25 nm to 35 nm.

48. The method of claim 46, wherein the thickness of said first semiconductor layer is greater than the thickness of said second semiconductor layer, and wherein the thickness of the third semiconductor layer is greater than the thickness of the second semiconductor layer.

49. The method according to claim 38, further comprising a step of forming an electrode layer above said third semiconductor layer and covering at least a portion of the first side of said ridge portion in the longitudinal direction, wherein the thickness of said electrode layer is equal to or more than 100 nm.